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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,099	03/01/2004	Eric Chen-Li Sheng	TRAN-P283	2474

7590 06/13/2005

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EXAMINER	
SUN, XIUQIN	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 06/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/791,099	SHENG ET AL.	
	Examiner	Art Unit	
	Xiuqin Sun	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 17-33* is/are rejected.

7)☒ Claim(s) *16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/18/04&03/21/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-14 and 19-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Chandrakasan et al. (U.S. Pub. No. 20040183588).

With respect to claims 1, 8 and 27, Chandrakasan et al. teach a computer-implemented method and computer software program that implements the method of reducing temperature variation among integrated circuits during burn-in testing, comprising: measuring power consumed by an integrated circuit under test (sections 0075, 0079 and 0121); measuring an ambient temperature associated with said integrated circuit under test (sections 0079, 0084 and 0131); and adjusting a body bias voltage of said integrated circuit under test to achieve a desired junction temperature of said integrated circuit under test (sections 0084, 0088, 0095 and 0121).

With respect to claims 2-7, 9-14, 20-25 and 28-33, Chandrakasan et al. teach: said ambient temperature is measured for a region comprising only said integrated circuit under test (sections 0043 and 0084); said ambient temperature is measured for a

region comprising more than one integrated circuits under test (sections 0044 and 0084); said measuring power comprises measuring current to said integrated circuit under test (section 0113); an operating voltage of said integrated circuit under test remains fixed during said measuring and said adjusting (section 0096); said body bias voltage is individually controllable for said integrated circuit under test (sections 0018 and 0086); said integrated circuit under test comprises body-biasing well structures to accept said body bias voltage (sections 0045 and 0060).

With respect to claim 19, Chandrakasan et al. teach a system for testing an integrated circuit comprising: an operating voltage supply for coupling said integrated circuit (section 0075); a current measuring device for coupling said integrated circuit for measuring operating current of said integrated circuit (section 0109); a body bias voltage supply for coupling said integrated circuit for
providing a body bias voltage (sections 0114 and 0121); an ambient temperature sensor for determining an ambient temperature for a region proximate to said integrated circuit (sections 0079, 0084 and 0131); a test controller for coupling said integrated circuit and coupling said current measuring device, said bias voltage supply and said ambient temperature sensor, said test controller for implementing a method for reducing temperature variation among an integrated circuit during burn-in testing, said method comprising (sections 0084, 0088, 0095, 0121 and 0122): accessing a measure of power consumed by said integrated circuit (sections 0075 and 0079); accessing a measure of ambient temperature associated with said integrated circuit (sections 0079, 0084 and 0131); and adjusting said body bias voltage of said integrated circuit to achieve a

desired junction temperature of said integrated circuit (sections 0084, 0088, 0095 and 0121).

With respect to claim 26, Chandrakasan et al. teach: said method implemented by said test controller also comprises stimulating said integrated circuit for testing (section 0122).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 15, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chandrakasan et al. (U.S. Pub. No. 20040183588) in view of Cohen et al. (U.S. Pub. No. 20050088137).

With respect to claims 15 and 18, Chandrakasan et al. teach a computer implemented method of determining a junction temperature of an integrated circuit, said method comprising: measuring an ambient temperature in a region proximate to said integrated circuit (sections 0079, 0084 and 0131); measuring electrical power utilized by said integrated circuit (sections 0075, 0079 and 0121); and determining a junction temperature of said integrated circuit (sections 0084, 0088, 0095 and 0121).

Chandrakasan et al. do not mention expressly: accessing a thermal resistance value for said integrated circuit; and said thermal resistance value is accessed from a computer usable media.

Cohen et al. disclos methods and apparatus for controlling the performance of integrated circuits having a thermal limitation, and teach: using a thermal resistance value of said integrated circuit for controlling the performance of said integrated circuit, and said thermal resistance value is accessed from a computer usable media (sections 0017 and 0018).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teaching of Cohen et al. in the invention of Chandrakasan et al. in order to consider the impacts of external factors such as the ambient temperature, and inherent features of the microprocessor technology, such as the thermal resistance to heat flow from the IC junction to the ambient air, on the performance of said integrated circuit (Cohen et al., sections 0017).

With respect to claim 17, the teaching of Chandrakasan et al. includes: said measuring electrical power comprises measuring current to said integrated circuit (Section 113).

Allowable Subject Matter

5. Claim 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for Allowance

6. The following is an examiner's statement of reasons for allowance:

The primary reason for the allowance of claim 16 is the inclusion of the claimed method step of multiplying said thermal resistance value by said electrical power and adding said ambient temperature. It is this limitation found in the claim, as it is claimed in the combination that has not been found, taught or suggested by the prior art of record, which makes this claim allowable over the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Prior Art Citations

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1) Butler (U.S. Pub. No. 2004018867) is entitled "System for and method of assessing chip acceptability and increasing yield".

2) Fan (U.S. Pub. No. 20040083075) is entitled "Junction temperatures measurements in semiconductor chip package technology".

Contact Information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Xiuqin Sun whose telephone number is (571)272-2280. The examiner can normally be reached on 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571)272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Xiuqin Sun
Examiner
Art Unit 2863

MICHAEL NGHIEM
PRIMARY EXAMINER

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May 24, 2005